WEST Refine Search Page 1 of 1

## **Refine Search**

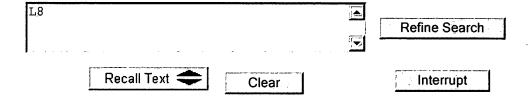
## Search Results -

Terms	Documents	
ASIC and ASSP and FPGA	111	

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

Database:



## Search History

## DATE: Tuesday, February 22, 2005 Printable Copy Create Case

Set Name side by side	Query	<u>Hit</u> Count	Set Name result set
DB = 1	PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR = YES; OP = OR		
<u>L8</u>	ASIC and ASSP and FPGA	111	<u>L8</u>
<u>L7</u>	(clock\$3 adj tree) and flip-flop and gate and (metal\$8 or interconnect\$3) and (custom\$3 or user)	215	<u>L7</u>
<u>L6</u>	(platform same silicon) and (clock\$3 adj tree) and flip-flop and gate and (metal\$8 or interconnect\$3) and (custom\$3 or user)	1	<u>L6</u>
DB =	USPT; PLUR=YES; OP=OR		
<u>L5</u>	L4 and clock\$3 and gate and flip-flop	380	<u>L5</u>
<u>L4</u>	L2 or L3	2574	<u>L4</u>
<u>L3</u>	716/7,10,12,13,14,16,17.ccls.	1950	<u>L3</u>
<u>L2</u>	257/202, 204-211.ccls.	662	<u>L2</u>
<u>L1</u>	716/7,10,12, 13, 14, 16, 17.ccls.	3264438	<u>L1</u>

END OF SEARCH HISTORY